CLASS-A/D APPROACH FOR
CMOS HIGH EFFICIENCY RF POWER AMPLIFIER

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B.E., Kyungpook National University, Korea 2001

A THESIS
submitted in partial fulfillment of the
requirements for the degree
MASTER OF SCIENCE
Department of Electrical Engineering and Computer Engineering
College of Engineering
KANSAS STATE UNIVERSITY
Manhattan, Kansas
2003

Approved by:

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ABSTRACT

The design of an integrated CMOS Power Amplifier (PA) for a Jet Propulsion Laboratory (JPL) Synthetic Aperture Radar (SAR) mission is studied. Although there are a number of PA class definitions and published circuits, designing a high efficiency RF PA is still a challenging job. In this thesis, the goal is full integration in Silicon-on-Sapphire (SOS) using on-chip spiral inductors/transformers. A number of PAs are paralleled and the transformers, which have secondary sides in series, link the outputs in order to expand the output power up to 5W Peak Envelop Power (PEP).

This thesis describes major classes of PAs and details class-D and class-E PAs. When the class-D PA is turned on more than half period, it improves virtual ground state in a differential amplifier structure providing immunity to bonding wire parasitic inductance problems. This modified class-D PA is named class-A/D. A class-E PA lacks bonding wire effects immunity. However, it has potential to decrease the number of transformers by using an output matching network. A representative, class-A/D 600 mW PA is designed and simulated in Agilent ADS. A differential structure gives a virtual ground to make the design immune to bonding wire parameters, and enables the PA to use center-tapped transformers. The transformers also link multiple output ports of PAs. The secondary spirals are connected in series such that low output voltage from each stage stacks up at the secondary. The simulated class-A/D PA has 660 mW output power, 51.6% drain efficiency and 45.3% Power Added Efficiency (PAE). A class-A/D 4-stage PA is also designed to output 5W PEP. This PA, compared to the previous 600 mW PA, does not degrade its performance seriously in simulation. The drain efficiency is 47.4 %, and PAE is 45.2 %.

A layout floor plan of the class-A/D 4-stage PA is provided as a basis for further development. JPL and Kansas State University will refine the design and add a balun in the full integration. The other circuitry for a complete Transmitter/Receiver (T/R) module is being developed simultaneously. Ultimately, all the circuitry will be mounted on a one-chip T/R module.
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Chapter 1

Introduction

1.1 Synthetic Aperture Radar

To examine a broad area, Synthetic Aperture Radar (SAR) is being used. It can be used for monitoring the environment, mapping geological resources, and military purposes [1] and can be boarded on an aircraft or on an artificial satellite.

![Figure 1.1: Constructing a synthetic aperture [2]](image)

An imaging radar illuminates a target area with radio waves, receives reflected signals and analyzes the data. It collects data in the direction that the radar is moving along. Then the system uses the Doppler effect to view this data as if it is collected from a large aperture, which means better resolution. The received signals are stored in order and a synthesizing process takes delays and Doppler effect into account and
recovers the signals. Since SAR transmits its own signals instead of receiving light from the target, it works regardless of weather conditions [2].

1.2 Flexible Membrane Antenna Application

Jet Propulsion Laboratory (JPL) in NASA is currently researching to develop a Flexible Membrane Antenna Technology for Radar Applications. The research will dramatically decrease the mass of the satellite approximately to one tenth, which is directly related to a decrease in the cost of the satellite. The technology can be applied to most SAR missions and be scaled to other frequencies up to Ka-band. The first step of the mission is to build a lightweight fold-up antenna. In a traditional Transmitter/Receiver (T/R) structure of the satellite, a large Power Amplifier (PA) feeds an array of patch antennas through a power divider. However, in this project, thousands of small-sized T/R modules are deployed directly upon an inflatable frame, which needs full integration of subordinate circuits including PA.

Since the project is supposed to have on-chip MMIC T/R module, the process must be reliable with diverse applications. CMOS process is the most flexible and even cost effective. Its high density integration and versatility handle analog, digital, and mixed signal circuits such as a signal processor, a signal converter and a memory. True system-on-a-chip design is possible in CMOS process [3]. In a space mission program, another concern is the ionizing radiation environment in earth orbit. It causes system errors on occasion and the hard error such as latch-up by the radiation that may destroy the system permanently. However, a Silicon-on-Insulator (SOI) process does not make parasitic bipolar transistors, so it is free from latch-up.

Among subordinate circuits to be included in the CMOS T/R module, PA is taken as a prime research subject because we found that there were not many literatures on an integrated PA in CMOS process. This thesis elaborates solutions in Silicon-on-Sapphire (SOS) process to attain a high efficient RF PA in single-chip form.

1.3 Thesis Outline

Chapter 2 explains prior art (past research work on integrated PA and on passive devices needed; specifically on-chip spiral inductors and transformers). A simple circuit model of a spiral inductor and the effects of quality factor on PA efficiency are given. Various transformer architectures are available using spiral inductors. Each architecture has both good and bad points. Using SOS process or an SOI process with high starting wafer resistivity (> 1 kΩ·cm) for transformers has some advantages such as low substrate loss and small substrate capacitance. Summary of published literatures on an integrated CMOS PA is also explained.

Chapter 3 describes the definition and performance of various PA classes. The PA classes are grouped into a current source mode or into a switch mode. Class-A, B and C amplifiers act as current sources and class-
D, E and F amplifiers as switches. The chapter gives more detailed discussion on class-D, E and F amplifiers.

Challenges in the fabrication are addressed in Chapter 4. Low gate-drain breakdown voltage in a high frequency CMOS process limits output power. In addition, to achieve enough gain, a large MOSFET is needed, which brings in a large gate capacitor as well. It causes matching problem at the gate input. An inductor between two differential RF inputs cancels the capacitor out. Finally, an RFIC package has some amount of inductance in bonding wires and leads. A designer must take care of this inductance. It is described how class-E power amplifier and class-A/D power amplifier are designed to achieve high efficiency and bonding wire immunity. The chapter provides the schematics of 600 mW PA and series-combined class-A/D 4-stage PA. It also presents the circuit simulation results for each class.

Chapter 5 provides conclusions and suggestions to complete the fully integrated T/R module.
Chapter 2

Prior Art

This chapter reviews the often-used components like on-chip spiral inductors and transformers, and prior work on integrated PAs and power combining techniques.

2.1 On-chip Spiral Inductor

In RF circuit design, many design difficulties come from the fact that the real inductor on chip has far lower performance compared to the ideal one. There are different sorts of categories of on-chip spiral inductors such as circular, square, and micro-machined inductor. But, the square inductor is the most commonly used and this section will focus on it.

![Figure 2.1: Square spiral inductor geometry](image)

In general, the square spiral inductor geometry can be expressed by four parameters, \(D\) (Dimension), \(S\) (Spacing), \(W\) (Width), and \(N\) (Number of turns). Figure 2.1 is surface geometry of the square inductor. At
low frequency, the basic values like inductance ($L$) and series resistance ($R_s$) can be extracted by simple formula [4]. Bigger dimension and more turns give higher inductance. The center third area contributes little inductance and is kept empty usually, and series resistance depends on the ratio of total trace length to the width and sheet resistance of metalization layers.

As the frequency becomes higher, the inductor analysis needs to consider more factors. $R_s$ is not constant because of current crowding effects in the metalization layers and losses in the substrate. When a magnetic field penetrates metalization layers and the substrate, it creates eddy current loops. The current flows in the direction that it opposes the magnetic field. The interaction is modeled as inductor-resistor loops and coupling coefficient, $k$. The eddy current effects become dominant as a frequency goes high [4], [5]. So, $R_s$, $R_{sub}$ in figure 2.2 are not constant but rather complex frequency dependent values. Between the layers, capacitors exist. $C_{ox}$ is an oxide capacitor, $C_p$ is a coupling capacitor between turns, and $C_{sub}$ is a capacitor between an oxide layer and ground metal.

![Spiral Inductor Circuit Model](image)

Figure 2.2 : Circuit model of spiral inductor

The quality factor ($Q$) of the inductor is
\[ Q = \omega \frac{\text{average energy stored}}{\text{energy loss/second}} \]  

(2.1)

If high frequency effects are negligibly small then \( Q \) can be calculated by two parameters \( L \) and \( R_s \).

\[ Q = \frac{2\pi \omega L}{R_s} \]  

(2.2)

Minimizing parasitic capacitance and series resistance and maximizing (or minimizing) \( R_{sub} \) in the inductor guarantees higher \( Q \). \( R_{sub} \) loss is minimized when the substrate resistance is around 20–50 Ohms or higher than 100 kOhms [4]. A simple method is to put a patterned ground shield under the spiral so that \( R_{sub} \) is effectively shorted out [6]. Another way is Micro-machining technology that can make air-gap between layer and substrate by substrate etching [7], but the process is too complex and expensive to be widely applied. An SOS process has high enough substrate resistance to promise competitive high \( Q \) inductor design and eliminate \( C_{ox}, R_{sub}, R_{sub-eddy}, \) and \( C_{sub} \) from the model of figure 2.2. In the SOS process, the primary loss is due to series resistance and current crowding (\( R_{eddy-trace} \)) effects [5].

### 2.2 On-chip Transformer

The mutual inductance between two spiral inductors makes them exchange power. This interaction through magnetic field delivers power without considerable loss and it keeps DC states on both primary and secondary side. These power coupling and bias independence properties have good advantages when the transformer is applied to design power amplifiers [8], [9], Gilbert Cell mixers [10], isolator designs [11] and so on.

A modified transformer circuit model of Cheung, et al’s low-frequency model [12] is shown as figure 3. Depending on primary to secondary distance and geometry, the coupling coefficient (\( k \)) varies. Parasitic resistor and capacitor of each inductor are shown as \( R_s, C_{res} \) and \( R_{sub} \). Since two inductors are closely located, there is also a coupling capacitor (\( C_c \)) between turns.
Transformers are designed for criteria such as symmetrical structure, higher $k$, and center-tap. The interwound transformer in figure 2.4 has symmetrical shape with the same number of turns. This feature is very desirable if the same electrical characteristics are required in both directions, and it has a moderate value of $k$ ($\approx 0.8$) [13].

The stacked transformer is composed of two identical metal layers in the different levels as shown in figure 2.5. This achieves better magnetic coupling ($k > 0.8$) between primary and secondary. But, the stacked
transformer has more significant coupling capacitance ($C_c$) than other structures [13]. To try to minimize this capacitor, primary turns can be placed with some offset from the secondary [14]. However, in either case, the $Q$ performance is compromised since top-layer (thick) metal cannot be used for one of the inductors.

The square symmetric transformer in figure 2.6 has the convenience that the primary and secondary edges are located at the opposite sides. This can be used as a balun too because it can be divided exactly into two halves at the electrical center point, or center-tap. By grounding the center of the primary or secondary it can serve as differential input, single output or vice versa [13].
2.3 Power Combining Technique

The output power of PAs has a quadratic relation with the drain voltage [15]. If output load is fixed at 50 Ohms, the drain voltage should be boosted in order to make required output power. However, MOSFETs are not able to sustain high drain voltage as the geometry is scaled down for high frequency operation, and low power consumption. As long as the supply voltage and the drain voltage are limited, some kind of output power combining technique is needed.

Assume one needs N PAs to get target output power. Transformers can connect N low drain voltage PAs in series (figure. 2.7). While the drain voltage at the primary side is lower than the breakdown voltage, the output current from the single PA is N times bigger since the PA maintains the drain voltage and sees only R/N. The output voltages from the primary sides add up at a secondary side because the transformers are connected in series. This is the technique applied in this research to obtain a 5 W PA in a 0.5 µm SOS process.

![Figure 2.7: Schematics of Parallel to Series PA](image)

2.4 Prior Integrated PAs

The list of prior work on integrated PAs is in table 2.1. The target frequency for integration is from 700MHz to 2.4GHz. Class-E PA design seems to be the most favored in the list because it avoids parasitic losses that arise during integration. A second harmonic tuning class-F PA was also designed and got 42% PAE. Contrary to the nonlinear trends, Chen’s fully integrated PA is a linear mode design and it shows
16% efficiency without LTCC (Low Temperature Co-fired Ceramic) inductor. From this, it is clear why the linear PA is not often adopted in high efficiency PA design. In theory a class-E PA is capable of 100% efficiency but the list shows that the real products end up at around 40% efficiency. Heinz’s and Sowlati’s designs get 50% but they use Si bipolar and GaAs processes respectively. Mertens’ puts two baluns out of a chip and it gets around 62%. In CMOS design they achieved 1W output power without any power combining technique. This thesis must consider the power combing technique as an important issue as it aims to 5W PEP output.

<table>
<thead>
<tr>
<th>Author</th>
<th>f0 (GHz)</th>
<th>P0 (W)</th>
<th>Class</th>
<th>Efficiency</th>
<th>Process</th>
<th>etc</th>
</tr>
</thead>
<tbody>
<tr>
<td>F. Fortes et al [16]</td>
<td>1.9</td>
<td>0.2</td>
<td>F</td>
<td>PAE=42%</td>
<td>0.6 µmCMOS</td>
<td>Off-chip output matching</td>
</tr>
<tr>
<td>K.Tsai et al [17]</td>
<td>1.9</td>
<td>1</td>
<td>E</td>
<td>PAE=48%</td>
<td>0.35µm CMOS</td>
<td>Differential, external balun</td>
</tr>
<tr>
<td>K.Mertens et al [18]</td>
<td>0.7</td>
<td>1</td>
<td>E</td>
<td>PAE=62%</td>
<td>0.35µm CMOS</td>
<td>Differential, two external balun</td>
</tr>
<tr>
<td>A.Heinz et al [8]</td>
<td>0.9</td>
<td>3.2</td>
<td></td>
<td>PAE=54%</td>
<td></td>
<td>Si bipolar</td>
</tr>
<tr>
<td>Yoo et al [19]</td>
<td>0.9</td>
<td>0.9</td>
<td>E</td>
<td>PAE=41%</td>
<td>0.25µm CMOS</td>
<td>Common-gate switching</td>
</tr>
<tr>
<td>Sowlati et al [20]</td>
<td>0.835</td>
<td>0.25</td>
<td>E</td>
<td>PAE=50%</td>
<td>0.8 µm GaAs MESFET</td>
<td>Class-F driver, Class-E PA</td>
</tr>
<tr>
<td>Chen et al [21]</td>
<td>1.9</td>
<td>0.25</td>
<td></td>
<td>η=16% 32% (LTCC)</td>
<td>0.8 µm CMOS</td>
<td>LTCC inductor</td>
</tr>
<tr>
<td>Aoki et al [22]</td>
<td>2.4</td>
<td>1.9</td>
<td>E/F_odd</td>
<td>PAE=41%</td>
<td>0.35 µm CMOS</td>
<td>DAT, Virtual ground</td>
</tr>
</tbody>
</table>

Table 2.1: Prior works of the integrated PAs

Ichiro Aoki’s study suggested a Distributed Active Transformer (DAT) for power combining [22]. Multiple power amplifiers are connected in series using on-chip transformers similar in concept to figure 2.7. In their design, shown in figure 2.8, no current is flowing directly from primary to secondary coils so that each power amplifier is isolated. Each stage can be either a single ended or differential PA. Although manipulating the turns ratio can transform the impedance viewed at the primary side, a 1:1 transformer is favorable because smaller turn ratio results in lower power loss. Changing the number of series connected amplifiers will change the output impedance of single amplifier and that will get rid of matching network. Furthermore, the split load impedance enables the low drain voltage to carry the required power. Apart from the general advantages of DAT, concerning the high loss of the spiral inductor on chip, it proposes to use a slab inductor. The circular geometry of transformer provides virtual ground and it is symmetrical in every corner of the amplifier. The author reported 1.9W output power and 41% Power Added Efficiency (PAE).
2.5 Silicon-on-Sapphire Process

Although a slab inductor was chosen to minimize transformer power loss in Aoki’s design, Silicon-on-Sapphire process provides competitive high-$Q$ inductors and transformers. The transformer composed of spiral inductors couples magnetic fields better than simple two square slab inductors. For those reasons, more traditional spiral transformers are chosen through the thesis.

In addition to eliminating possible parasitic capacitance in circuits, its low substrate loss property gives a solution to a high-$Q$ inductor problem. Currently $Q$ of higher than 40 at 2GHz is reported [23]. Considering the spiral inductors in bulk CMOS process has the $Q$ of less than 10, this process breaks the limitations from the poor inductors in RF design. GaAs process also aims at similar improvements but SOS process provides feasible cost and simple design.
Chapter 3

Power Amplifier Classes

So far, more than ten classes of power amplifiers have been introduced. If little modified versions are included, organizing all the classes is out of the question [24]. Thus, this thesis will deal with generally well-known classes and those directly relevant to integrated L-band design. Class-A, B, and C amplifiers have the same topology and they are referred as linear mode amplifiers or current source mode amplifiers, but they have different bias conditions to enhance power efficiency.

Just a scaled up small signal amplifier with a resonant load does not give a good solution to high efficiency RF power amplifier, so different methods should be devised [25]. Class-D and E PAs suggest using the transistor as a switch instead of a current source. Ideally, these amplifiers have 100% power efficiency since they satisfy a zero voltage switching condition [26]. A class-F PA with a λ/4 transmission line also behaves as a switching PA. If the transmission line is not available, it improves power efficiency by adding one or more harmonics resonant circuits. The class-D, E and F PAs sacrifice linearity in order to obtain better power efficiency.

Before examining the classes, the power efficiency should be defined. The most common definition is drain power efficiency ($\eta$), or just efficiency. It is the ratio of RF output power to input DC power.

$$
\text{efficiency, } \eta = \frac{P_{\text{RFout}}}{P_{\text{DC}}}
$$

(3.1)

In the case that RF input power is significant, the drain efficiency is not capable of giving an idea about power efficiency. Power Added Efficiency (PAE) is more useful since it takes the input RF power into account. The PAE is the ratio of RF output power minus RF input power to input DC power.

$$
\text{Power Added Efficiency} = \frac{P_{\text{RFout}} - P_{\text{RFin}}}{P_{\text{DC}}}
$$

(3.2)
Another frequently used term is normalized power output capability ($P_{max}$). $P_{max}$ is the maximum RF output power available when 1 V maximum drain voltage and 1 A maximum current are applied. Actual output power capability can be estimated by multiplying $P_{max}$ by the drain maximum voltage and the maximum current [27].

3.1 Class A, B, and C Power Amplifiers

Class A, B and C are so called linear modes or current source modes. As the transistor acts like a current source, the drain voltage does not saturate when it is on and by this reason the RF output power is proportional to the RF input power [24]. All the linear mode classes are derived from the same circuit topology of figure 3.1. DC power is supplied to the drain through a RF Choke (RFC) inductor. Because this inductor is large enough ($L_{RFC} \geq 10L$), the current fed is assumed constant. $C_b$ blocks DC current from the transistor. A parallel resonant circuit is loaded with $R$. The resonant circuit has high enough $Q$ that a signal or harmonic out of the bandwidth goes to a ground through the resonator. Only the frequency of interest is loaded on the $R$.

3.1.1 Class-A Power Amplifier

A Class-A PA is the larger model of a traditional small signal amplifier. Figure 3.1 is the exact class-A PA without any modification. A bias condition is set for the transistor to operate linearly with input signal such that the transistor is always in an active region. Here, we assume that threshold voltage and drain saturation
voltage are negligible and RFC is infinite. So, the drain voltage swings from zero up to $2V_{DD}$. To see how effectively this circuit can carry input power to the load, drain current is expressed by

$$i_D = I_{DC} - I_{D,\text{peak}} \sin \omega t, \quad I_{D,\text{peak}} = \frac{V_{DD}}{R}$$

(3.3)

$I_{DC}$ is the DC bias current, $I_{D,\text{peak}}$ is the maximum peak amplitude of RF signal, and $\omega_0/2\pi$ is the resonant frequency of the tank circuit. The drain voltage is

$$v_D = V_{DD} + V_{D,\text{peak}} \sin \omega_0 t$$

(3.4)

The ac voltage has opposite sign to the ac current since drain current decreases as the current to the output increases, and $V_{D,\text{peak}}$ is same as $V_{DD}$ in ideal high efficiency conditions. $C_b$ eliminates the DC part from $v_D$. Thus,

$$v_o = \frac{V_{o,\text{peak}}}{R} \sin \omega_0 t, \quad V_{o,\text{peak}} = V_{D,\text{peak}}$$

(3.5)

![Figure 3.2 : Class-A PA waveforms](image)
To keep the transistor in active region, the bias current is always supplied, which predicts poor efficiency. The efficiency is calculated quantitatively. Under the ideal conditions $I_{D,\text{peak}}=I_{DC}$ and $V_{o,\text{peak}}=V_{DD}$ shown in figure 3.2. The DC input power is then

$$P_{DC} = V_{DD}I_{DC} = \frac{V_{DD}^2}{R}$$  \hspace{1cm} (3.6)

The RF output power is

$$P_{O} = \frac{V_{o,\text{peak}}^2}{2R} = \frac{V_{DD}^2}{2R}$$  \hspace{1cm} (3.7)

Therefore, the maximum drain efficiency of Class-A PA is

$$\eta = \frac{P_{O}}{P_{DC}} = \frac{1}{2}$$  \hspace{1cm} (3.8)

50% of efficiency is not bad for power amplifier but this number is ideal. Once realistic factors such as inductor power loss and on-resistance are considered, ending up 15% of power efficiency is not surprising [25].

We can see how much output power is available for a given device or process by inspecting the normalized power output capability ($P_{\text{max}}$).

$$P_{\text{max}} = \frac{P_{RFout}}{V_{D,\text{max}}I_{D,\text{max}}} = \frac{V_{DD}^2}{(2V_{DD})(2V_{DD}/R)} = \frac{1}{8}$$  \hspace{1cm} (3.9)

So, if the CMOS PA can withstand 6 V drain-source voltage ($V_{D,\text{max}}=2V_{DD}$) with 50 Ohms load, then $I_{D,\text{max}}$ is 120 mA ($\approx 2V_{DD}/R$) and approximately 90 mW output power is possible with a 3V supply and no matching network.

3.1.2 Class-B Power Amplifier

In a class-A PA, the bias condition lets current always flow through the transistor and results in low power efficiency. A Class-B PA maintains the bias condition such that the transistor is on for half a cycle. A push-
pull configuration can be used if a center-tapped transformer connects the drains of two transistors. Below is the derivation with the assumption of a single-ended PA case. The drain current is

\[
\begin{align*}
    i_D &= \begin{cases} 
    I_{D,\text{peak}} \sin \omega_0 t, & 0 < \omega_0 t \leq \frac{T}{2} \\
    0, & \frac{T}{2} < \omega_0 t \leq T
    \end{cases}
\end{align*}
\]  

(3.10)

With a resonant circuit, only the fundamental frequency is carried to the load and it is the output current \(i_0\). By Fourier expansion, the output current is

\[
I_{O,\text{peak}} = \frac{2}{T} \int_0^\frac{T}{2} I_{D,\text{peak}} (\sin \omega_0 t)(\sin \omega_0 t)dt = \frac{I_{D,\text{peak}}}{2}
\]  

(3.11)

\[
i_D = I_{O,\text{peak}} \sin \omega_0 t = \frac{I_{D,\text{peak}}}{2} \sin \omega_0 t
\]

(3.12)

Because the drain voltage can swing up to \(2V_{DD}\), the voltage at a load swings from \(+V_{DD}\) to \(-V_{DD}\) and \(I_{D,\text{peak}}\) is \(V_{DD}/R\).

Figure 3.3 : Class-B PA waveforms
Output power can be calculated

\[ P_o = \frac{V_{dd}^2}{2R} \]  

(3.13)

The \( P_o \) is same with class-A’s. DC current from a supply cannot go to the load so the DC input current is equivalent with DC current through the transistor.

\[ I_D = \frac{2}{T} \int_0^{\frac{T}{2}} I_{D,\text{peak}} \sin \omega_0 t \, dt = \frac{2}{\pi} I_{D,\text{peak}} = \frac{2V_{dd}}{\pi R} \]  

(3.14)

The DC input power is

\[ P_{DC} = I_D V_{dd} = \frac{2V_{dd}^2}{\pi R} \]  

(3.15)

Finally, the drain efficiency is

\[ \eta = \frac{V_{dd}^2 / 2R}{V_{dd}^2 / \pi R} = \frac{\pi}{4} \approx 0.785 \]  

(3.16)

While the transistor is turned on for half a period, the power efficiency increases to 78.5 % from 50 % for class-A. \( P_{\text{max}} \) for the class-B PA does not change from that of the class-A PA for the reason that maximum drain voltage and current remain same.

### 3.1.3 Class-C Power Amplifier

The class-B PA obtains higher efficiency by decreasing the time that the transistor is on. A class-C PA develops this idea further and the transistor is on for less than half a period.
When the drain current is trimmed, the lower part of the sinusoid is off. With a conduction angle of $2\gamma$ we can derive $\eta$ and $P_{\text{max}}$ such as \[ \eta = \frac{2\gamma - \sin 2\gamma}{4(\sin \gamma - \gamma \cos \gamma)} \] (3.17)

\[ P_{\text{max}} = \frac{2\gamma - \sin 2\gamma}{8\pi(1 - \cos \gamma)} \] (3.18)

Theoretically 100% efficiency is achieved when $\gamma$ approaches zero. Unfortunately, however, $P_{\text{max}}$ then approaches zero because maximum drain current rises infinitely.

Among the studied literatures Y.J.E. Chen experimented with the current source mode PA [21]. It is a two-stage cascade PA, which has one stage for maximum voltage gain and the other stage to boost maximum power. Due to full integration, the PA’s power efficiency is capped at 16%. Although the mode can give better linearity, low power efficiency is a primary reason why a switch mode is favored for high efficiency RF applications. And for switch mode applications, linearization techniques are under development to recover the signal from distortions.

3.2 Class-D, E and F Power Amplifiers
Class D, E, and F assume that a transistor operates as a switch. In this case, during part of cycle the transistor is considered as open circuit and during the rest part it is a short circuit with an ideally zero on-resistance. When the switch is on, the voltage across it should be minimized to keep power loss low. Using a large sized transistor is one way. But, area efficiency should be considered and the large transistor always engages troublesome gate capacitance.

### 3.2.1 Class-D power amplifier

A Class-D PA is an implementation of the idea that if the transistor switches on and off perfectly then no power is wasted through the transistor. Commonly a push-pull structure with a transformer is favored. If it maintains constant voltage at the center of the transformer’s primary side, it is defined as a voltage-switching class-D PA. In the other case, if constant current is supplied through the RFC as illustrated in figure 3.5, it is a current-switching class-D PA. Both types have similar characteristics except whether voltage or current plays the switching role and what type of resonant circuit is used. The voltage switching requires the fundamental frequency be band-passed through a series resonant circuit. The other PA uses a parallel resonant circuit to filter out harmonics.

![Figure 3.5: Current switching class-D PA](image)

Since the current switching employed in class-D is similar to that in the final design of this thesis, it is detailed below.
From the $V_{DD}$ supply the constant current flows through $M1$ and $M2$ alternately. As the transformer ratio is set at 1:1, when M1 turns on, only half the coil is effective at the moment. So, turn ratio at the time is 1:2 and current ratio is 2:1. The resulting $i_{sd}$ in the secondary is a square wave, which peaks from $1/2 \, i_{DC}$ to $-1/2 \, i_{DC}$. Only a fundamental frequency of the current reaches the load, $R$.

The various voltages and currents are found to be:

$$i_{sd} = \frac{i_{DC}}{2} \frac{4}{\pi} \left( \sin \omega_0 t + \frac{1}{3} \sin 3\omega_0 t + \frac{1}{5} \sin 5\omega_0 t \ldots \right)$$  \hspace{1cm} (3.19)

$$i_o = \frac{i_{DC}}{2} \frac{4}{\pi} \sin \omega_0 t$$  \hspace{1cm} (3.20)

$$v_o = \frac{i_{DC}}{2} \frac{4}{\pi} R \sin \omega_0 t$$  \hspace{1cm} (3.21)

To compute DC power consumption, one should know $i_{DC}$. Since the voltage at the center of primary winding is $v_o/2$ and is a fully rectified signal, its average must be $V_{DD}$.

From 3.21,

$$V_{DD} = \frac{1}{2} \frac{2i_{DC}}{\pi} R T \left( \int_0^T (\sin \omega_0 t) dt - \int_0^{T/2} (\sin \omega_0 t) dt \right) = \frac{2i_{DC}}{\pi^2} R \frac{T}{2}$$  \hspace{1cm} (3.22)

Hence,

$$i_{DC} = \frac{V_{DD}}{2R} \frac{\pi^2}{2}$$  \hspace{1cm} (3.23)

and the output power is

$$P_o = \frac{V_{DD}^2 \pi^2}{2R}$$  \hspace{1cm} (3.24)

As can be seen in figure 3.6, either voltage or current is always zero. Hence, there is no power loss at the transistor and power efficiency is 100%.
In a real class-D PA, perfect switching is not realizable. Before the drain current becomes zero, drain voltage starts to grow because a stray capacitor is charged. This problem escalates as the frequency goes up. The loss is mainly from an overlap capacitor between the drain and source. The capacitor is repeatedly charged and discharged when the transistor turns on and off. This power in the capacitor does not help any of output power and deteriorates power efficiency. Despite these problems, the current switching class-D PA has some important advantages useful in the application targeted in the thesis. The transformer inductor can share the role of a RFC since they are connected in series and the transformer can make up a parallel resonant circuit. As the resonant capacitor is moved into the primary part, the secondary coil is more flexible for the sake of layout when connecting multiple stages.

3.2.2 Class-E Power Amplifier

N. O. Sokal and A. D. Sokal introduced a class-E PA to address imperfect voltage transition and capacitor loss [28]. This PA exploits the reactance of a loading circuit so that it can keep the drain voltage at zero
when the switch transistor turns on. \( C_{\text{shunt}} \) includes the unwanted overlap capacitor of the transistor as a necessary circuit element.

![Class-E PA schematics](image)

Here, the transistor switches on and off by \( v_I \). The \( L-C \) series circuit can be seen as the combination of an \( L_o-C_o \) resonant circuit tuned to the fundamental frequency and a supplementary reactance as shown in figure 3.7. The resonant circuit makes a sine wave and the latter shapes \( v_D = 0 \) and \( i_c (= C_{\text{shunt}}d v_D/dt) = 0 \) at the turn-on transition as shown figure 3.8. Therefore, at the transition, the energy stored in \( C_{\text{shunt}} \) is not consumed through the transistor and power loss is minimized.
Figure 3.8 : Class-E PA waveforms

A little complicated equation solving is needed at this point. Quoting the paper [28], the circuit component values can be derived.

\[
Q = \frac{\omega L}{R} \quad (3.25)
\]

\[
X = \frac{1.110Q}{Q - 0.67} R \quad (3.26)
\]

\[
B = \omega C_{\text{shunt}} = \frac{0.1836}{R} \left( 1 + \frac{0.81Q}{Q^2 + 4} \right) \quad (3.27)
\]

With these components, output power and peak drain voltage are

\[
P_o = 0.577 \frac{V_{dd}^2}{R} \quad (3.28)
\]

\[
v_{D,\text{peak}} \approx 3.56V_{dd} \quad (3.29)
\]
For fully integrated designs, the endurance against breakdown should be considered. Large $V_{DD}$ cannot be used since $v_{D,peak}$ is typically limited to less than 6 V in high frequency CMOS process, and due to the high $v_{D,peak}$ class-E PA’s $P_{max}$ is small.

Although the idea is introduced in single mode, a differential mode using positive feedback was tried for a couple of integrated CMOS circuits with high power efficiency. K. Tsai’s circuit has 48% PAE [17], and K. Mertens’ has 62% PAE [18] (with addition of external balun).

### 3.2.3 Class-F Power Amplifier

A class-F PA has two different types. One type uses a third harmonic frequency $L$-$C$ resonant circuit between the drain and a load. Here, a transistor’s behavior is like a current source or a saturated current source. The other type uses a $\lambda/4$ transmission line to create multiple odd harmonic resonators and the transistor is regarded as a switch. Although if a transmission cannot be used on-chip at the frequency of interest, it is briefly explained.

Figure 3.9 is a simple schematic of a class-F PA with a harmonic resonant circuit. As the transistor supplies sinusoidal current during the half cycle that the class-B PA does, the third- harmonic resonant tank circuit $L_3$-$C_3$ is seen as a short by drain current going to the load because of the tank circuit $L_o$-$C_o$ output $v_o$ is sine wave with fundamental frequency. As for drain voltage, it sees the load at the fundamental frequency and an open circuit at the third harmonic frequency respectively. The drain voltage is therefore sum of fundamental and third harmonic frequencies. When the amplitude of third harmonic frequency is one ninth of the amplitude of fundamental frequency, the waveform is maximally flat (figure 3.10).

The third harmonic frequency resonator can be replaced by resonators for every odd frequency. Then, $v_D$ looks like a square wave because the square wave has only odd harmonics when it is expanded by Fourier series.
A class-F PA with a $\lambda/4$ transmission line that accomplishes this objective is shown in figure 3.11. If impedance of transmission line is $Z_0$ and $Z_0$ is equal to load impedance ($Z_0 = R$), the output impedance seen at a drain is $R$ at $f_o$. At the other harmonic frequencies, $C_o L_o$ circuit acts as a short to ground. At odd harmonic frequencies, the shorted end is converted to open circuit by the lines, and the drain sees only the output impedance of the transistor itself. As a result, $v_D$ is shaped to a square wave as seen in figure 3.12.
T. Sowlati uses the class-F concept for a class-E PA’s driver amplifier. First and third harmonic resonant circuits at the drain make square wave input to the PA [20]. An integrated second harmonic tuned class-F PA is also demonstrated by F. Fortes et al [16]. A bonding wire and an off-chip capacitor are used for output matching. Output power is 200 mW and PAE is 42%.

Figure 3.11 : Class-F PA with a $\lambda/4$ transmission line

Figure 3.12 : Class-F PA with a $\lambda/4$ transmission line waveforms
Chapter 4

Class-A/D and Class-E Power Amplifier: Design and Simulation

A class-A/D PA is designed. The PA is expanded to 2-stage and 4-stage differential PA using the proposed transformer power combining technique. A class-E PA does not have as strong bonding wire immunity as the class-A/D. However, class-E PA has potential to reduce the number of transformers by using matching network, which results in the less number of PA stages. A harmonic tuning class-F PA was not tried because it needs more inductors, which cause more power loss.

4.1 Class-A/D Power Amplifier

4.1.1 Introduction

A major concern in PA design is parasitics of power and ground bonding wire. A class-D current switching PA has natural tolerance of this problem and is suggested as the core of the transformer-based PA of figure 2.7.

A prototype design was first aimed to operate at 1.2 GHz and to output 600 mW. Two center-tapped transformers are used to connect outputs of two differential mode amplifiers in series.
The circuit topology follows that of a current switching class-D PA which assumes constant supplying current from $V_{SS}$ and high $Q$ resonant circuit at the output. An inductor is picked to give enough circuit $Q$ and small series resistance loss. And p-channel transistors are placed instead of n-channel transistors since breakdown measurements proved p-channel transistors could withstand higher voltage.

Without an infinite RFC, the supply current is not constant when a sine wave is given instead of a perfect square wave as switching input (figure 4.2.1). If the bias is given as $V_{SG} = |V_t| + \alpha$ ($\alpha > 0$) and the transistor is turned on more than half a period (figure 4.2.2), the current fluctuates less and gets closer to ac ground (figure 4.2.3). This virtual ground increases the output power without increasing supply voltage and improves power efficiency, too. Because of the different bias from the conventional class-D PA, the circuit will be named class-A/D PA.
Due to the large size of the transistor, its capacitive gate has small impedance at 1.2 GHz and pulls in significant current to the gate. When the RF input is supplied from a 50 Ohms transmission line, the voltage loading on the line lowers the amplitude of switching RF input. The input matching inductor ($L_{m}$) reduces these adverse effects.

### 4.1.2 Simulation Results

Although a classic interwound spiral transformer has better coupling, it is hard to locate the electric center point in the interwound transformer structure. So, the transformer in the simulation uses a square symmetric structure as seen in figure 4.4 and the primary inductance is about 50 % bigger than the secondary. The capacitance between the primary and the secondary layers is also modeled. $C_{ex}$ and $R_{sub}$ are not modeled
since the transformer’s self resonant frequency is much higher than $f_o$ and $R_{sub}$ is very high. A simulation confirmed that these parasitic capacitors did not cause any degrading results with high secondary voltage. The simulation was executed in Agilent ADS. Realistic transformer $Q (=15)$ was assumed. Its schematic is attached in Appendix.

DC power supplied is 1.28 W, RF input power is 80 mW, and RF output power yields 660 mW. Drain efficiency is therefore 51.6 %, PAE is 45.3 % and $P_{max}$ is 0.32.

![Simulation Waveforms](image)

Figure 4.3 : Class-A/D PA simulation waveforms

### 4.1.3 Circuit Layout

The original circuit design and simulation were done assuming that the PA would be fabricated in SOS FC process that provides high quality inductors ($Q=15$). Prior to laying out for FC process, the layout for SOS FA process was tried. For the output coupling, two square symmetric transformers are used. The
transformer traces are 3 layers stacked for low series resistance and the inductor $Q$ is expected to be lower ($=10$) in this process. In the output resonant circuit, MMM capacitors are used so that either FA or FC process can be used, when the circuit is fabricated.

Figure 4.4 : Class-A/D PA layout
4.2 Class-A/D 4-stage Power Amplifier

4.2.1 Introduction

To expand output to the target 5 W PEP output, four differential PAs need to be linked in series. The 50 Ohms antenna loads 12.5 Ohms upon each differential pair. That brings some changes of circuit parameters. The $L-C$ output tank circuit and the matching inductor ($L_m$) values are adjusted to compensate Miller’s capacitor and the increased input capacitor.

![Class-A/D 4-stage PA schematics](image)

Figure 4.5: Class-A/D 4-stage PA schematics

4.2.2 Simulation Results

The simulation is done assuming inductor $Q$ is 15 and transformer $k$ is 0.7, which is the same hypothesis as the previous design. The output power is 3.5 W (7.1 W PEP). The drain efficiency is 47.4 %, PAE is 45.2 % and $P_{\text{max}}$ is 0.56.
4.2.3 Layout Floor Plan

The layout is not a multiplied replica of the 600 mW class-A/D PA because the quarter of the load is allotted to the each differential pair at this time. To decide on a new transformer value, one should keep in mind that a low inductor-series-resistor ($R_s$) plays a key role in improving power efficiency. Hence, two one-turn circular spiral inductors are used to compose a transformer and the matching inductor also has one turn and a wide layer. $Q$ is higher but smaller coupling is expected. Even if the transformers are located to let the current flow to the same direction and oppose magnetic field against one another, their magnetic interference is negligible. Prior studies [29] show one tenth of inductor dimension is enough separation to isolate inductors.

Figure 4.7 is the layout plan for the class-A/D 4-stage PA.
4.3 Class-E Power Amplifier

From the literature, it is shown that a class-E PA should be a suitable circuit for the 5W PEP PA of the SAR mission. Since the project does not require linear output to the RF input, the maximum efficiency is the major interest. Class-E PA’s superior power efficiency is well known for it switches at zero drain voltage and absorbs transistor overlap capacitor into its circuit parameter.

At first, a single PA is tested. The simulated schematic is the same as figure 3.8, which is repeated in figure 4.8 with component values shown.
Basic class-E PA needs low resistance load to get desired $P_{out}$ at low voltage. If we do this, then the series $R-L$ circuit forms a matching network that allows load to be 25 Ohms but circuit to see the needed 0.62 Ohms (figure 4.8). When transformers connect two parallel $R-L$ circuits to make a differential pair, the total output impedance becomes 50 Ohms. $Q$ of 5 is used when the class-E circuit values are calculated ($L_o = 0.41$ nH, $Q = \omega_o L_o / R$). But, when the circuit in a dotted box (figure 4.9) is replaced with transformer circuit, the $Q'$ of series circuit is 6 because the $L$ value is the sum of the $L_o$ and supplementary inductance $X/\omega$. It is not reasonable to increase $R_s$ as long as $Q$ should be at least 5 for sinusoidal output signal. Otherwise, converted $R_p$ is more than 25 Ohms and multiplication of PAs cannot match a 50 Ohms antenna without any kinds of impedance transforms.
Under the ideal conditions, the drain voltage stays at the minimum before the switch turns on. But, in reality, the minimum voltage is not zero because of a transistor’s on-resistance. The simulated waveforms of the figure 4.8 circuit are shown in figure 4.10. Although the size of the transistor increases further to give more current, $v_D$ saturates at about 9 volts, which is 84% of the theoretical value. Likewise the output power also does not reach the theoretical value.

The schematic of the differential class-E is presented in figure 4.11. As shown in the figure 4.9, the resistor is moved to the secondary side and joined in series.

Figure 4.10 : Class-E PA simulation waveforms
Without a bonding wire inductor at the bottom, this circuit works as expected in the theory. But, when it is fabricated, the bonding wire effects cannot be ignored. The length of bonding wire is not fixed and its inductance varies from 0.5 nH to 5 nH depending on its package. So, the bonding wire inductor is added to the schematics in the second simulation. While $\eta$ was 67.5% without the bonding wire, $\eta$ was 67.0% with 0.5 nH minimum bonding wire and 63.5% with 0.8 nH wire. However, when the circuit is simulated with 1 nH bonding wire, the voltage at the common source does not keep constant and the PA did not have any power gain. As the power the PA handles increases, so do the bonding wire effects. To relieve the adverse effects, a by-pass resonator is suggested (figure 4.12). Since the current through the bonding wire has doubled frequency, $2f_o$, the circuit is sized to resonate at $2f_o$. This method can eliminate the problem but there is a practical concern that $L_{2b}$ should be much less than $L_{bondwire}$ not to divide the voltage at the common source. Unfortunately, in that case, $L_{2b}$ is too small to be laid out accurately.
After the speculation on class-E PA, it is concluded that the PA should be accompanied with a better solution of the bonding wire effects. Another problem is high drain voltage ($=3.56V_{dd}$), which can cause transistor breakdown. Scaled-down high frequency CMOS processes cannot withstand such high voltage. In addition, the design in figure 4.11 is hard to output different levels of output power because the practical value of the minimum inductor is limited at 0.5nH, which prevent smaller $R_s$ for more stages. Conversely, a bigger $R_s$ for less output power makes a bigger $R_p$, which needs impedance transform for the 50 Ohms antenna application. However, this design decreases the number of transformers due to the output matching network. So, a solution for the bonding wire effects is still needed.
Chapter 5

Conclusions

5.1 Conclusions

This thesis presented a high efficiency RF PA for a JPL’s SAR mission. Various PA classes were studied. A differential class-E PA on-chip design was examined. The circuit’s performance was degraded when bonding wire effects are included but it could decrease the number of transformers since output matching network enables the PA to have low impedance load. A differential class-D PA was simulated and it had strong bonding wire immunity. A class-A/D increased the time that a transistor is on to enhance power efficiency. A 600 mW class-A/D PA was designed and simulated. It provided 51.6% drain efficiency and 45.3% PAE. A power combining technique is realized by connecting multiple transformers. An expanded 4-stage class-A/D PA was also designed and simulated. It had 47.4 % drain efficiency and 45.2 % PAE.

The results demonstrate that a high efficiency RF PA can be accomplished in CMOS SOI or SOS process. Furthermore, this PA design provides a cheap, bonding wire effects free PA solution to the SAR mission.

5.2 Future Works

The class A/D PA is not a fully integrated on-chip design. Its differential structure needs a balun at the input. Addition of the on-chip spiral balun will complete a fully integrated PA design. The design should be fabricated in either SOI process or SOS process to see the anticipated operation. Prior to fabrication of the design, various on-chip transformers should be tested and confirmed.

Research of a low noise amplifier and a T/R switch is going on to realize a complete on-chip T/R module.
REFERENCES


Appendix

Agilent ADS Schematics: Class A/D 600mW Power Amplifier