DC Test Theory
DC Parametric Test Items

- Test done by precision measure unit (PMU)
- IDD Leakage
- Input parameters: VIH, VIL, IIH, IIL
- Output parameters: VOH, VOL, IOH, IOL
- Power consumption test: Static, Gross, & Dynamic Idd
**Open/Short Test**

**Procedure**

- Ground all pins (including VDD)
- Using PMU force -100 uA, one pin at a time
- Measure voltage
- Fail open test if the voltage is less than -1.5 V
- Fail short test if the voltage is greater than -0.2 V
Open/Short Test Q & A

- Why does device have 2 diodes?
- Why we test only GND side diode usually?
- Why we use FIMV mode to test O/S normally?
- Why we test O/S before any other test items?
- When you setup a tester, you find a specific DUT which fail at open. How can you find out the root cause?
- When you setup a tester, you find a specific DUT which fail at short. How can you find out the root cause?
Input Leakage Low Test (IIL)

**Procedure**
- Apply VDDmax
- Pre-condition all input pins to logic ‘1’ with PE
- Using PMU force Ground to individual pin
- Wait for 1 to 5 msec
- Measure current
- Fail IIL test if the current is less than –10 uA

![Diagram](image_url)
**Input Leakage High Test (IIH)**

**Procedure**
- Apply VDDmax
- Pre-condition all input pins to logic ‘0’ with PE
- Using PMU force VDDMAX to individual pin
- Wait for 1 to 5 msec
- Measure current
- Fail IIH test if the current is greater than +10 uA

**Diagram**
- PMU
  - 5.25V
  - 0.00mA
  - Measure
- VDDmax
  - Force
- VSS=0
  - Sense
  - IIH
- VLSI
- PEs force logic 0
  - On all input pins

**Results**
- GT 10uA
  - Fail IIH
  - Pass
Output Voltage Test (Voh/Ioh)

**Procedure**
- Apply VDDmax
- Pre-condition all output pins to logic ‘1’
- Using PMU force IOH current per specification
- Wait for 1 to 5 msec
- Measure voltage
- Fail VOH test if the voltage is less than +2.4 uA
Output Voltage Test (Vol/Iol)

Procedure
- Apply VDDmax
- Pre-condition all output pins to logic ‘0’
- Using PMU force IOL current per specification
- Wait for 1 to 5 msec
- Measure voltage
- Fail VOL test if the voltage is greater than +0.4 uA

GT 0.4V
- Fail VOL
- Pass
Output Short Circuit Test

**PMU**

<table>
<thead>
<tr>
<th>0.0V</th>
<th>force</th>
</tr>
</thead>
<tbody>
<tr>
<td>-52.4mA</td>
<td>Measure</td>
</tr>
</tbody>
</table>

**VDDmax**

**VLSI**

**Procedure**

- Apply VDDmax
- Pre-condition all output pins to logic ‘1’
- Using PMU force 0V
- Wait for 1 to 5 msec
- Measure current
- Fail VOL test if the current is outside the limit range

**GT - 30mA**
- Pass

**LT - 85mA**
- Fail Short Circuit
Static Idd Test

**Procedure**

- Using DPS or PMU to apply VDDmax on power pin
- Execute Pre-condition pattern
- Stop pattern
- Wait for 1 to 5 msec
- Measure current flowing into VDD pins
- Fail Isb test if the current is greater than Isb spec. (Normal in uA)
**Gross Idd Test**

**Procedure**
- Using DPS or PMU to apply VDDmax on power pin
- Set Pass/Fail limit
- Set all input pins Low/High or Execute reset sequence
- Stop pattern
- Wait for 1 to 5 msec
- Measure current flowing into VDD pins
- Fail Isb test if the current is outside IDD gross spec.
Dynamic Idd Test

PMU

5.25V
force

12.4mA
Measure

force

sense

VDD

VLSI

Vss=0

Procedure

• Using DPS or PMU to apply VDDmax on power pin
• Execute Pre-condition pattern
• Wait for 10 msec
• Measure current flowing into VDD pins while device is executing pattern
• Fail I sb test if the current is greater than IDD spec. (Normal in mA)
• Stop pattern

GT IDD spec

Fail Dynamic IDD

Pass