The Process and Challenges of a High-Speed DUT Board Project

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Abstract
This paper addresses the overall project needs and recommended project practices for a high-speed ATE interface. The interface between the device under test (DUT) and the test system is typically referred to as a DUT Board or Loadboard (herein referred to by Loadboard). The goal of developing a high-speed loadboard is to maintain high signal integrity on those signal lines where it is critical to the performance of the device, and accurate testing. This paper will focus more on project management, and fabrication issues in implementing a high-speed design and less on high-speed design techniques. High-speed design techniques will be touched upon as needed to illustrate the key message. The goal of this paper is to complement other design techniques based papers and provide a complete picture of a Loadboard activity.

High-Speed Loadboard Project Process

Introduction
The DUT interface is becoming much more critical to accurate testing than ever before. Emerging high speed devices like SerDes, SONET, Hypertransport, LVDS, TMDS, etc. put severe performance requirements on ATE, especially the interface. Simply laying out a textbook 50 Ohm transmission line is no longer adequate. A high signal integrity loadboard for high-speed (or high frequency) requires much more complex and high level design techniques than would have been required a few years ago.

Figure 1 illustrates the signal path and issues at each point along the path. Any single element can be a Signal Integrity killer. Most people are beginning to realize this and are seeking out expert design guidance. However, executing the desired design as a finished board in one Fab cycle, at a reasonable cost, and utilizing less than ideal PCB process is just as important.

Development Segment
Many years ago, in a much lower frequency world, loadboards were a simple point to point wiring exercise to connect test resources to DUT pins. This could be accomplished with wire-wrap or simple

![Diagram of loadboard signal path and issues](image)

Figure 1, Idealized loadboard signal path and issues
PCB construction techniques. This activity justified itself as a straightforward technician level task. As frequency increased the technician was forced to layout a simple transmission line using simple lossless transmission line calculators. However, it still remained a straightforward technician level exercise, even if the responsible engineer contracted an outside service. Today's high-speed boards require a far more serious project management approach. The basic elements of a loadboard project are illustrated in figure 2.

![Figure 2, Loadboard Project Process](image)

The most critical phases in this process are the first three, Investigate, Specify and Design. Let's first establish that the goal of any project is to achieve the highest performing deliverable result, with the lowest investment, and shortest reasonable schedule. In the case of a loadboard, schedule delays due to mistakes in these first three phases (figure 3) can lead to huge

![The Relative Cost of Correcting Errors Through the Development Lifecycle](image)

Figure 3, It is less expensive to catch errors early. [1]

cost over-runs in terms of both material scrap and delays in production ramp which could exceed $1M dollars ($700k loss example shown in figure 4).

Errors that cause an impact on performance effect tester accuracy and ultimately product yields. Again these have huge implications on the customer's overall product development and production ramp

![Cash Flow (Profit) for New Device](image)

**Assumptions**
- 500,000 devices per month
- 9 months of production
- Same endpoint for both scenarios
- $20 part price / 10% profit
- 30%/yr price erosion
- 16% discount rate

Figure 4, Lost revenue as a function of delayed product ramp. This example, net loss of delay: $784k.
costs. It is a well known principle that errors which slip unnoticed through the early phases of any project produce huge costs and delays in the later phases.
The complexity of the device, tester, and high frequency design issues, demand a serious project approach to this activity.

The critical questions that need to be answered first for each process phase are:

- What is the necessary deliverable at each phase?
- Who is responsible for creating the required deliverable?
- What is the hand-off to the next phase?

The three most probable parties to be involved are:
- customer
- tester vendor (Sales Rep. & App. Engr.)
- 3rd party service(s) (design, layout, Fab., etc.)

In addition, the engineering detail can be broken into roughly two classes:
- basic electrical engineering and layout definition for the lower-speed lines
- RF design and layout definition of the high-speed lines

It must be clear from the onset of the project who is managing the overall project and who is responsible for the individual phases. Failure to do so produces errors that result in rework. It doesn't matter who performs these functions so long as they are qualified and understand their responsibilities. The one party with the most to lose, and therefore bears ultimate oversight, is the customer. Therefore, the customer should ensure that these roles are satisfied. For example, the customer might assume responsibility for the investigation, specification and the low frequency portion of the design. The customer may choose to subcontract the high frequency design activity and eventual layout activity to external consultants and design service vendors. This is clearly a valid plan so long as all parties clearly understand their roles and responsibilities.

The most common mistake is when a low-end engineering service or layout person is contracted and expected to perform high-end RF design. The resulting mismatch in scope, expectations and responsibilities will produce delays, scrap, and rework.

Investigation, Specification and Design Phases
The following process practices ensure success at each phase. As noted in figure 2, there are specific outputs at the end of each phase:

- Project Request Form
- Statement of Work
- Design Document & Layout Package

In addition the Design Phase ends with a successful Design Review Checkpoint, and all known issues or concerns addressed.

The Project Request Form in its most basic form needs to clearly identify the device; its pin-out, the tester and its resources, any critical signal paths or functions, and a requested delivery date.

The Statement of Work (SOW) in its most basic form, needs to clearly articulate the effort that will be performed to realize the appropriate loadboard design, including the design techniques and construction techniques to be employed. It should include a detailed schedule and target cost. The biggest CAUTION here is to keep a clear distinction between research and product development in the development of deliverables and schedule. It is a common practice in the industry to try new technologies on the customer's loadboard at the customer's expense. This is valid if it is part of the overall proposal and agreed to by the customer. It is unacceptable if the customer is expecting a finished board, performing to specification within a defined schedule. However, high-speed and high frequency is an unknown world that will require research. Intermediate experimental boards are recommended if the performance needs exceed what's possible with known practices. Such experimental boards should be factored into the Statement of Work and clearly communicated to all parties, most especially the end customer.

The Layout Package is the output of the Design Process. Typically the package is comprised of three documents:

- General layout design rules
- Test system manufacturer specific mechanical guidelines
- Project specific requirements

Together these documents need to clearly describe the goals, needs and constraints of the design. The package needs to describe all of the critical signals and the layout criteria for those signal traces. General mechanical information, such as keep-out areas or other layout information specific to docking also needs to be included.

Another very important process activity is "Engineering Change Control". Once the SOW is bought-off as the official "plan of record", and especially after the Design Review checkpoint, all changes to the design, construction plan or other critical plans must be documented and communicated to all parties involved. The typical document that is used is called an Engineering Change Notice. Various forms of this have been around for decades. The most critical part is that it documents the change, the reasons for the change, the implications for the change to other parts of the project, and who is to be notified.

Opportunity for Designer
The designer can greatly contribute to the project success by becoming familiar with the Fab process. The ideal loadboard PCB process would be one that is easy to perform and takes relatively little time; the dielectric materials have very low transmission loss; the overall cost is very low; and for which very dense high speed circuits signal traces are possible. It is said that high-speed loadboards want thin-film performance at FR4 PCB processing prices.

No such process exists.

Everything about the project is a compromise. The more the designer understands both the layout tools and Fab process the better able the designer is able to make trade-offs between performance, cost and yield. The designer is then able to add more value to the program by recommending changes to the original specifications that might have a minimal effect on performance and huge effect on costs or manufacturability.

Another important contribution the designer can make is to become familiar with the various high frequency simulation tools. Significant cost and time can be saved by simulating structures and calibrate

Figure 5, Example 10Gbps test board for proving high-speed design techniques.

those structures against measured s-parameter results on test boards called coupons (figure 5). Thus the designer is able to build up a library of different

Figure 6a, VIA study: Model and TDR simulation.
structures and Fab techniques for future reference (figure 6). Beware of SPICE macro-models. These might make good approximations after the fact, but SPICE is a 2-dimensional lumped element simulation and not a distributed 3-dimensional field solver. For fundamental investigations the more advanced simulators are actually a cost savings.

![Diagram](image)

Figure 6b, DUT and Pogo Via model to 6.5 mil stripline, model and TDR eye-diag. simulation.

**Execution Segment**

The next segment in the overall Project Management process is the Execution Segment. The three phases that comprise this segment have a strong vendor management theme because in almost all cases the project will utilize external service vendors and subcontractors. These next three phases are:

- Layout
- Fab
- Assembly

Service vendors for these functions are critical to the overall loadboard project and industry in general. They provide a lower cost service than if the customer staffed his/her own internal department, and because they handle multiple similar projects, they are able to maintain a higher level in certain skills. However, they do need to be well managed and provided the right information, "garbage in is garbage out". They are not a part of either the customer's organization or the ATE vendor's organization and are disconnected from those communication paths. It is recommended that the overall project manager conduct weekly or biweekly project meetings during the course of the project to ensure everyone gets the information required for the execution of their task.

**Layout Phase**

The Layout phase ends with a Layout Review and the output is:

- a set of Gerber files,
- Stackup
- Assembly Drawings

The layout review is a very critical phase in that this is the last chance to correct any serious mistakes before major Fab expenses and schedule commitments are incurred. For example, if the final stackup includes inner layers of FR4 to reduce cost, then double check that the rise time or frequency specification for the signals on those inner layers can be achieved in FR4.

**Fab Phase**

The project manager and designer should familiarize themselves with the process limitations and ensuing costs of the selected vendor's Fab process. The kinds of things that can go wrong during the Fab Phase in a high-speed, non-FR4 loadboard project are the following:

- Inability to achieve a 50Ohm ± 5% transmission line due to stack-up and other manufacturing factors.
- Excessive scrap due to thin non-FR4 dielectrics
- Failure to meet performance goals due to Fab modifications to Gerber files.
- Excessive scrap and rework due to using high-speed dielectric materials that are inappropriate for low volume loadboard projects.
- Excessive scrap or rework or falling short on performance specifications due to tight geometries, narrow diameter drills, high layer counts, and soft materials. Pushing the envelope of PCB Fab capabilities.
- Excessive cost or low performance due to not understanding the trade-offs with skin effect, density, frequency, and cost.

Typically, loadboard projects don't have the luxury of multiple proto runs like a high volume standard product would have. The following suggestions will help ensure success with a limited board run:

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• Understand what kinds of processing the Fab can reliably do and specify those for your loadboard project.

• Require that the Gerbers not be modified by the Fab, and request an explanation for any Fab yield concerns. For example, a 30mil relief in the ground plane from the edge to save saws may not sound like a big deal, but it does have a big impact on 10Gbps launch (see figure 7).

Figure 7a, Cross section diagram of edge launch with 30mil ground relief

• Typically loadboards utilize what is called an Asymmetrical stackup. This is required for ground plane, power plane and decoupling reasons. Ensure that your Fab can handle asymmetrical stackups which are prone to warping. (figure 8).

• High speed loadboard projects desire substrate dielectrics with low return loss. However, most of the best materials are difficult to work with requiring high volume per design to develop enough experience. The typical loadboard Fab does not command this kind of volume and the resulting experience. The following materials

• have proven the best for loadboard projects:
  • Getek/Nelco 4000-13
  • Rogers 4350 & 4003

• Avoid temptation to expedite the process. Rushing a board build generally increases the probability for error resulting in scrap for these otherwise difficult to build boards.

Figure 8a, Asymmetrical stackup illustration, typical of Loadboard, prone to warping.
Acceptance Segment
This segment is the final stretch of the process where we will determine the success or failure of the project. The phases in this segment are:

- Assemble Testing
- Installation
- Application Testing
- Final Acceptance Buy-off

Finished boards can not benefit from the kinds of test technology available to high volume PCB-based products. Most shops are not going to invest in board test systems for low-volume high-mix boards. Consider that less than 5 physical copies will be produced for a typical loadboard design. Also the very nature of a loadboard dictates that certain kinds of high-frequency parametric tests are required in addition to typical "opens and shorts".

In many cases the test plan needs to be determined during the design phase and any required fixturing is developed prior to the scheduled need.

Assembly Testing
Initial testing of the final assembly needs to be performed by the Assembler or Design House. It will involve verifying the construction was correct as per the layout and Fab instructions. It does not verify the functionality of the design or suitability to the target application, which will come later. During assembly testing the test plan should cover verification of the following items:

- Continuity of all connected pads, signal traces, lands, and components.
- Opens between connected pads, signal traces, lands, and components.
- Shorts between unconnected pads, signal traces, lands and components.
- Correct value of all soldered-down components.
- Correct impedance value of sample transmission lines.
- Correct component, fit and assembly of all mechanical components.
- Correct construction and finished parameters of any critical performance areas

Installation
During installation the correct mechanical fit both:
- within the test system or "test head"
- as well as with a handler docked (if handler use is planned)
should be checked and verified acceptable to intended use. Improper component clearance or mechanical stress can cause premature failure in high-use production environments.

**Application Testing**
This is the point that performance and suitability to application is determined. The test engineer will have developed a tester specific application program for the DUT. The test plan will generally cover the following key test groups:

- Continuity
- Supply currents
- Functionality testing at speed

Test results that require documentation are device family specific, but would generally be:

- Shmoo plots
- Rise and fall time measurements (with ATE or scope as appropriate)
- If mixed-signal or RF, then appropriate frequency measurements to correct harmonic content.
- Whatever other pass/fail or performance information to demonstrate that the loadboard is performing correctly with the DUT, and ATE system. It is important to note that the objective is to test the loadboard and look for design or manufacturing faults in the loadboard. Both the DUT and ATE system are assumed to perform correctly unless proven otherwise. Therefore, any testing that might be a normal part of the DUT test plan can be omitted if it bears no significance on the check-out of the loadboard.

**Final Acceptance Buy-off**
There will always be parts of the loadboard that could be better, and even some mistakes that can be solved with external modifications, but at some point a final conclusion needs to be reached and the appropriate vendors paid for their services. An Acceptance Plan should be included as part of the initial SOW and purchase agreement. It does not need to include all possible tests. It should include those tests that both parties agree will demonstrate that the final product meets the original (or modified through ENC) requirements of the purchase agreement and design.

- The end customer needs to ensure that the loadboard is serviceable and doesn't suffer from poor workmanship or poor design practices.
- The service vendor(s) need to guard against creeping features, and customers who simply don't know what they want.

This is a contractual purchase issue and should be decided upon before the design phase.

**Summary**
The above discussion could apply to any hardware or software development project. Indeed the basic project management concepts are widely published and available from numerous sources. It has proven to be especially important with high-speed and high-frequency loadboard projects for the Agilent 93000 SOC test system. Projects always suffer delays and cost overruns in cases where this process was ignored by either Agilent personnel or subcontractors. When coupled with a solid foundation in high-speed or high-frequency design, layout and Fab techniques, a loadboard that meets the technical requirements can be realized in the shortest time and lowest cost.

This is probably the end of the discussion for leading edge loadboard applications intended for the engineering and characterization phase of semiconductor product development. There still remains the question of production loadboard applications where manufacturing is far more sensitive to cost and delivery issues. There is a growing concern with the growing cost of test tooling for today's main-stream products [2]. The mismatch in expectations will become more severe as high-speed and high-frequency products enter main-stream production. Looking forward the industry is faced with several challenges and questions:

- Cost increasing with speed, will customers pay?
- Design cycle time increasing with speed, will customers pay?
- What is the future of high speed production test?
- Is this another production issue that will be taken over by BIST, with true high speed testing left as a lab activity?
- This isn't just a test problem. It is also a device application problem. Will future device architectures reduce the actual speed requirement, and reverse the current trend?

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References
