The ADV212 and its Evaluation Card

Combining Analog Devices’ Superior Image Compression Technology with Xilinx’s Best-in-Class FPGA-Based Bus and Memory Management
Presentation Subjects:

- How you can use the Analog Devices ADV212 JPEG2000 compression engine to obtain a competitive advantage in your video market.

- How Analog Devices has the whole signal chain covered from “encode” to “decode.”

- How Analog Devices uses Xilinx FPGA’s in our video compression evaluation boards.

- How Analog Devices evaluation boards can help you in your entire product development cycle.

- How you can benefit from using Xilinx FPGA’s in a similar manner in your final product.
Important Points to Take Away

- Follow the money.
  - Know your video product’s market life cycle before you start designing.
  - Consider how product life cycle can impact technology choices.

- Plan your interfaces carefully.
  - Mixing video and “supervisory” interfaces can have disastrous consequences for video throughput.

- Recognize the pacing item on your project.
  - Hardware is commonly not the pacing item in video projects any more.
  - Software can often define the end date.

- Be aware that Xilinx offers reconfigurability and proven IP.
  - Many common housekeeping functions are available.

- Know that Analog Devices has done much of the video compression and transport firmware for you already.
  - The ADV212 comes ready to run the JPEG2000 compression algorithm.
Brief Overview of JPEG2000

- Next generation still and moving image compression standard from the JPEG Committee (members include: Kodak, Sony, Canon, Matsushita, HP, Sharp, Ricoh, Adobe, Nokia, Ericsson, etc.)
- Designed to address the shortcoming of JPEG including:
  - Better image quality:
    - Up to 50% better Pixel SNR performance than JPEG
    - Lossless compression possible
    - Compresses continuous tone (natural images) and bi-level compression (text) equally well
  - Scalability - dynamic bandwidth / quality control possible
  - Better error resilience compared to JPEG and MPEG
  - Content-based description and image security (encryption, copyright info, etc)
- No user fees for JPEG2000 (unlike MPEG4)
Image Comparison: JPEG2000 and JPEG Picture (50:1)
## Compression Comparisons

<table>
<thead>
<tr>
<th></th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Motion JPEG</strong></td>
<td>Most popular standard (cheapest to implement?); low process latency; used successfully in court</td>
<td>Least efficient compression compared to others; obvious degradation with any bit error; Unsuitable for text; no scalability</td>
</tr>
<tr>
<td><strong>MPEG2/4, H.264</strong></td>
<td>Ideal for streaming (very efficient compression, especially H.264); simpler decode process than encode; prevalent PC standard</td>
<td>Complicated encoding (MPEG4 / H.264); long process latency; weak error resilience (transmission errors affect multiple frames); License and user content fees for MPEG4; no still image capability (legal implications); not ideal for video editing; very limited scalability</td>
</tr>
<tr>
<td><strong>JPEG2000</strong></td>
<td>Low process latency (ADV202); better compression efficiency than JPEG; complete scalability; bit-error resilient; lossy/lossless capable; suitable for text and images</td>
<td>Less compression efficient than MPEG (ex: DVD-quality-VERY rough estimate: 10-12Mbps (JPEG2000); 8-10Mbps (MPEG2); 4-6Mbps (MPEG4))</td>
</tr>
</tbody>
</table>
**JPEG2000 Compression**

**First stage: 2D Wavelet Transform**

- High pass and low pass filters are applied to rows and columns, producing four subbands.
- Process is repeated on the “low low”, or LL subband.
- The LL subband is the most important for recreating the image.
- Other subbands provide detail and resolution.

*Courtesy of Michael W. Marcellin and Ali Bilgin – University of Arizona*
JPEG2000 Compression
First stage: 2D Wavelet Transform

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**JPEG2000 Compression**

**First stage: Wavelet Transform**

- High pass and low pass filters are applied to rows and columns, producing four sub-bands.
- Process is repeated on the “low low”, or LL sub-band.
- Very light quantization of all the frequency components in each transform level and each sub-band.
- Compressed to ½ to 1/3 of original size.
- Only step for lossless.

“Resolution Packet” size is dependent on image content.
JPEG2000 Compression
Second stage: Entropy Encoding

- Four parameters (Resolution / Quality Layer / Component / Precinct) can be hierarchically selected during the encoding process
- Possible because sub-bands are divisible into “layers”

In the case of Resolution Scaling (RLCP)
How LRCP Can be Used – Precise Rate Control

- Select packets to fill channel
- Almost all of the image quality is retained at half of the visually lossless bit-rate (~10:1)
- Note that rate control is also possible in RLCP or any other configuration
- Applications:
  - Wireless / Wired applications
  - Surveillance (variable HDD storage)

JPEG2000 Compression

- 40 Mbps
- 20 Mbps
- 10 Mbps
- 5 Mbps (with packet header)
JPEG 2000 Handles High Bit Error Rates*
(Compression ratio of 80:1, BER of $10^{-4}$)

Error Manifestation
High Frequency

JPEG2000 Compression

An error here

might look like this
Error Manifestation
Mid Frequency

An error here might look like this
Error Manifestation
Low Frequency

JPEG2000 Compression

An error here

might look like this
Where is JPEG2000 being used now?

- **Digital Cinema Initiative (DCI)**
  - Deployed in thousands of theatres as part of the recommended media for cinema distribution

- **Professional Video and Cameras**
  - Thomson’s Infinity™ Digital Media Camcorder and Recorder
  - The new emerging standard in pro video
  - Broadcast control rooms

- **Security DVR**
  - Designed into major security companies all over the world

- **Still image standard for various public institutions:**
  - Drivers License photos (Japan)
  - Various archiving applications (Library of Congress)
  - Medical imaging (DICOM)
  - Satellite photography
  - Military surveillance
JPEG2000 in Surveillance

Simultaneously transmit different resolutions, frame rates, and quality levels with no transcoding

- **Highest quality** image recorded for detailed review afterward
- **Medium quality** image for monitoring at base
- **Low quality** image for mobile monitoring (for lower transmission bandwidth via wireless)
Why Consider JPEG2000 when there is MPEG or H.264?

- **More flexibility** - encode at the highest quality but only use portions that fit the display media (resolution, frame rate, etc.) or to accommodate lower transmission bandwidth
  - Encode once; decode many different ways
- **Low latency** – essential in remote access (camera, channel, etc)
- **Higher image quality**
  - MPEG is not conducive toward high image quality since it is 8-bits only and has no still image capability
  - In the case of surveillance, JPEG2000 decimation (reducing frame rates from 30 fps to 1fps) files are ½ the size of MPEG2 decimation files (and better image quality) because decimated MPEG2/4 is motion JPEG.
- Easier frame-by-frame editing (for pro video)
- Multiplex between various cameras (for surveillance)
**JPEG2000 Benefit Summary**

- **Practical Real-time Compression**
  - Very high image quality – most efficient I-frame compression algorithms available
  - High resilience generation loss compared to JPEG / MPEG

- **Dynamic Bit-Rate Management**
  - Inherent resolution and quality scalability - provides optimal lower-resolution/quality proxy video without a separate codec
  - Precise bit rate control
  - Adjustable bit rate post-compression

- **Robust in the Presence of Transmission Errors**
  - No blocking artifacts
  - No error propagation between frames
  - Selective packet protection

- **Low Latency**
  - Instant remote control response
  - Simplified audio sync

- **No License Fees**
For More Information on JPEG2000

- Look for information on the “Mallat Transform.”
  - *A Wavelet Tour of Signal Processing*, Stephane Mallat
    - ISBN 0-12-466606-X

- Read ADI application note AN-576 *Using the ADV-JP2000*.
  - The app note is available for free download at [www.analog.com](http://www.analog.com).

  - The standard is there - along with many useful links.
The Misguided Chip Designer’s World View:

“Look what I did in silicon.”

“Here’s my chip on a board.”

“My evaluation board is also my silicon test fixture.”
How Things Go Wrong in Product Development

- Spin that board now...
- ...and think about software/firmware later.
- Reinvent wheels now thinking you can gain a few pennies later.
  - You probably won’t...
  - ...but you *will* guarantee that somebody’s in the market before you are.
How Things Go Right

- Recognize that software is usually the pacing item.
  - It’s also the least predictable as far as scheduling.

- Start coding on solid evaluation hardware.
  - Make sure your silicon vendor actually has solid evaluation hardware.
  - Make sure you’ve got decent software tools support.
    - Debuggers and Embedded Monitors
    - Emulators
    - Software Simulators
    - Disassemblers for Logic Analyzers
    - Linker/Locators, Libraries/Library Management Tools, and Support for Macros

- Keep hardware reconfigurability in mind.
  - You will encounter something you forgot in your hardware – so make sure you can go back and correct for the omission.
Our Objectives with the ADV212

- Compress Video / Save Bandwidth.
  - Full motion video is a notorious bandwidth hog.

- Provide Reasonable Interfaces.
  - "No Glue."

- Make Driver Development Easy.
  - Straightforward register arrangement means straightforward driver development.

- Save Customer Hassle of Doing Ugly DSP Development.

- Save Customer from Having to Have Intimate Knowledge of Compression Schemes.

- Be Cost Effective.
  - Again, "No Glue."
ADV212 Internal Architecture

ADV212

Pixel I/F
- Pixel I/F
- External DMA Ctrl
- Pixel FIFO
- Code FIFO
- ATTR FIFO

Wavelet Engine
EC1
EC2
EC3

Internal Bus and DMA Engine

Embedded RISC Processor System

RAM

ROM
The Xilinx FPGA-Based Memory Controller and DMA Engine
A Ready-Made I2C Slave from Xilinx

CoolRunner CPLD I2C Bus Controller Implementation

Summary

This document details the VHDL implementation of an I2C controller in a Xilinx CoolRunner™ 256-macrocell CPLD. CoolRunner CPLDs are the lowest power CPLDs available, making this the perfect target device for an I2C controller. To obtain the VHDL code described in this document, go to section VHDL Code Download, page 19 for instructions. This design fits both XPLA3 and CoolRunner-II CPLDs. For the CoolRunner-II CPLD version, please refer to XAPP385, CoolRunner-II CPLD I2C Bus Controller Implementation.

Introduction

The I2C bus is a popular serial, two-wire interface used in many systems because of its low overhead. The two-wire interface minimizes interconnections so ICs have fewer pins, and the number of traces required on printed circuit boards is reduced. Capable of 100 KHz operation, each device connected to the bus is software addressable by a unique address with a simple Master/Slave protocol.
A DMA engine from Xilinx

CAST, Inc.
IP Center,
75 N. Broadway
Nyack, New York 10960 USA
Phone: 1-845-353-6160
Fax: 1-845-768-7697
E-Mail: info@cast-inc.com
URL: www.cast-inc.com

Features

- Supports Virtex™-II, Virtex-E, Virtex, and Spartan™-II FPGAs
- Enable/Disable control of individual DMA requests
- Four independent DMA channels
- Independent auto-initialization of all channels
- Memory-to-memory transfers
- Memory Block initialization
- Address increment or decrement
- Directly expandable to any number of channels
- End of process input for terminating transfers
- Software DMA requests
- Independent polarity control for DREQ and DACK signals
- Functionality based on the Intel 8237

AllianceCORE™ Facts

<table>
<thead>
<tr>
<th>Core Specifications</th>
<th>Provided with Core</th>
</tr>
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<tr>
<td>Documentation</td>
<td>Core documentation</td>
</tr>
<tr>
<td>Design File Formats</td>
<td>.ngo, EDIF Netlist, VHDL Source RTL available extra</td>
</tr>
<tr>
<td>Constraints File</td>
<td>C8237.ucf</td>
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<tr>
<td>Verification</td>
<td>VHDL Testbench</td>
</tr>
<tr>
<td>Instantiation Templates</td>
<td>VHDL, Verilog</td>
</tr>
<tr>
<td>Reference designs &amp; application notes</td>
<td>None</td>
</tr>
<tr>
<td>Additional Items</td>
<td>Simulation and synthesis scripts</td>
</tr>
</tbody>
</table>

Simulation Tool Used

- 1076-compliant VHDL simulator

Support

Support provided by CAST, Inc.

Applications

The C8237 core is designed to improve system performance by allowing external devices to directly transfer information from the system memory.
An SDRAM controller from Xilinx

DDR2 SDRAM Memory Interface for Spartan-3 FPGAs
Author: Karthikeyan Palanisamy

Summary
This application note describes a DDR2 SDRAM memory interface implementation in a Spartan-3 device, interfacing with a Micron DDR2 SDRAM device. This document provides a brief overview of the DDR2 SDRAM device features, followed by a detailed explanation of the DDR2 SDRAM memory interface implementation.

DDR2 SDRAM Device Overview
DDR2 SDRAM devices are the next generation DDR SDRAM devices. The DDR2 SDRAM memory interface is source-synchronous and supports double-data rate like DDR SDRAM memory. DDR2 SDRAM devices use the SSTL 1.8V I/O standard.

DDR2 SDRAM devices use a DDR SDRAM architecture to achieve high-speed operation. The memory operates using a differential clock provided by the controller. (The reference design on the web does not support differential strobes. Support for this is planned to be added later.) Commands are registered at every positive edge of the clock. A bi-directional data strobe (DQS) is transmitted along with the data for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during reads, and by the controller during writes. DQS is edge-aligned with data for reads, and center-aligned with data for writes.

Read and write accesses to the DDR2 SDRAM device are burst oriented. Accesses begin with the registration of an active command and are then followed by a read or a write command. The address bits registered coincident with the active command are used to select the bank and row to be accessed. The address bits registered with the read or write command are used to select the bank and starting column location for the burst access.
ADV212 Evaluation Board
(Available Fall, 2007)
A Typical ADI Video Decoder
**Video Formats for Which ADI Anticipates Providing Encoder/Decoder Cards**

- ITU-R BT.656
- SMPTE 125M PAL/NTSC
- SMPTE 274M
- SMPTE 293M (525p)
- ITU-R BT.1358 (625p)
- SMPTE 274M HDTV (1080i)
- SMPTE 296M (720p)
- HDMI/DVI
- Component YCbCr/RGB
- HD/SDI (SMPTE 292M)
<table>
<thead>
<tr>
<th>Connectors We’re Using on the Daughter Cards</th>
</tr>
</thead>
<tbody>
<tr>
<td>1080i/720p (Y, Cb, and Cr).</td>
</tr>
<tr>
<td>HDMI-style 19-pin.</td>
</tr>
<tr>
<td>DVI-A, DVI-D, or DVI-I.</td>
</tr>
<tr>
<td>HD/SDI 75-ohm terminated.</td>
</tr>
<tr>
<td>S-video.</td>
</tr>
<tr>
<td>RCA-style for composite baseband video.</td>
</tr>
<tr>
<td>“Classic” 15-pin analog D-sub.</td>
</tr>
</tbody>
</table>
Possible Use for ADV212 Evaluation Boards
Case Study: Wireless HDMI

Using the Xilinx Spartan 3 with the ADV212 for wireless HD video
Wireless HDMI Product Architecture

HDMI/HDCP Tx

HDMI/HDCP Rx

JPEG2000 Encode

Packetization, AES128 encryption

Wireless Tx

HDMI/HDCP Tx

JPEG2000 Decode

De-packetization, AES128 decryption

Wireless Rx

HDMI/HDCP Rx

YCbCr

audio

audio

Spartan 3

Backchannel for control, HDCP repeater management

HDMI + HDCP
ADI – Tzero Wireless HDMI Configuration

**ADI Components**
- HDMI RX and TX, Power, Clocking, JPEG2000 Compression, Audio ADC/DAC

**Xilinx Spartan 3**
- PCI, AES128 Encryption, Buffer management, I2C, SPI, Stream Merge

**Tzero**
- UWB Radio, System Host
System Pieces

- HDMI
  - RX – ADV7443
  - TX – AD9389
- JPEG2000
  - ADV212 x 2
- Audio
  - AD1871 Audio A/D
  - AD1859 Audio D/A
- Spartan 3
  - PCI Master/Slave/Arbitration, Encryption, I2C, SPI, etc.
- Tzero UWB Radio
AircableT FPGA Block Diagram
AircableT FPGA Block Descriptions

- **PCI Arbiter**
  - Very simple, after boot up the Radio is always given the bus

- **Video Data Buffers**
  - Circular buffers, Headers identify the frame and sequence of the video data which is encrypted

- **AES128 Encryption**
  - Merged video data is encrypted before being placed in the video data buffers

- **Audio Buffers**
  - I2S Audio data is accumulated and stamped with a matching frame ID

- **I2C**
  - I2C Master allows the host to program the HDMI parts

- **ADV212 Host Control & Stream Merge**
  - Bridges the ADV212 Host bus to the PCI
  - Merges Luma and Chroma data into a single compliant JPEG2000 codestream

- **IR Blaster**
  - Takes data from the receiver side and drives an IR LED, used to extend IR remote controls for the source devices
AircableR FPGA Block Diagram

- PCI Bus
- PCI Arb
- Buffer
- AES Decrypt
- ADV I/F
- ADV CTL
- Audio buffer
- IR data RX
- Status/Clock Ctrl
- I2C Mstr
- ICM Buf
- Boot SM
- AFR
- ADV202s
- I2S to AD9889
- IR Receiver
- AD9989, EEPROM
AircableR FPGA Block Descriptions

- **PCI Arbiter**
  - Very simple, after boot up the Radio is always given the bus

- **Video Data Buffers**
  - Circular buffers, Host writes video data into them as they become available

- **AES128 Decryption**
  - Merged video data is decrypted before being sent to the decompression engine

- **Audio Buffers**
  - I2S Audio data is written here and then clocked out to HDMI and the DAC

- **I2C**
  - I2C Master allows the host to program the HDMI parts

- **ADV212 Host Control**
  - Bridges the ADV212 Host bus to the PCI

- **IR Receiver**
  - Takes data from standard IR remotes and converts it to a data stream to be sent to the TX board
Toolchain

- **RTL Source: Verilog**
  - Most blocks written in-house by ADI IC Designers
  - AES128 purchased from Helion
  - PCI Core purchased from Xilinx

- **Simulation: Synopsis VCS**
  - Same tool used in-house for IC Simulation

- **Synthesis: Synplicity Pro**
  - Expensive, but it was believed that it would provide more efficient output

- **Place & Route: Xilinx ISE**
  - Final step before MCS generation
Lessons Learned

- Create and keep Spec documentation up to date
  - Multiple people working as a team, spec is only control
  - Creating specification documents prior to Verilog coding uncovered many incorrect assumptions

- Trust (simulation), but VERIFY
  - All blocks had test benches and were simulated
  - In every case, simulation repeatedly failed to account for real-world cases
  - Simulation is necessary, but not sufficient to prove a block works

- Read the logs!
  - Many issues were found that were tool configuration problems
  - The Xilinx tools produce massive logs and critical information is scattered among hordes of useless stuff so pay attention.
Questions / Comments
RF to bits and back:
High-performance High-Speed Signal Processing Solutions

Analog Devices Inc.
April 2007
Agenda

- Analog Devices’ coverage of the Wireless signal chain
- Types of Wireless Architectures
  - Superheterodyne
  - Direct Conversion
  - IF Sampling
- Our solutions dovetailing into FPGA:
  - Design considerations vs. ADI Specifications
    - RF Amplifiers, VGAs, Mixers, Modulators, Demodulators, ADCs & DACs, Clocks and PLLs, RF Power Control
- Questions and Comments

www.analog.com/xfest07
Covering the Wireless Signal Chain: RF → Bits

Superheterodyne Architecture
Direct Conversion Architecture: Tx and Rx

Zero IF Rx

Zero IF Tx
IF Sampling and IF Synthesis

IF Sampling Rx

IF Synthesis Tx

www.analog.com/xfest07
Amplifiers...
RF Amplifiers

Key Design Considerations
- Low noise
- High linearity – IP3
- Output Power – P1dB
- Gain flatness

New RF Amps from Analog Devices
- Noise figure from 2dB
- Linearity: OIP3 upto +44 dBm
- Output Power, P1dB up to +27dBm
- Supply current as low as 23mA and in small LFCSP packages.

- LNA – Low Noise Amplifier
- Driver Amps
- IF Amps
- General Purpose Gain Blocks

ADL5322-23
ADL5541/42
ADL5530
ADL5531/2/3/4

www.analog.com/xfest07
Mixers...
RF Mixers

Key Design Considerations
- Low noise
- Frequency Range
- High linearity
- Conversion Gain/Loss

High IP3 Mixer
- Low Freq to 4GHz
- IIP3 of +26 dBm
- -6dB conversion loss
- 6dB noise figure

www.analog.com/xfest07
Variable Gain Amplifiers…
Variable Gain Amplifiers

Key Design Considerations
- Frequency Range
- Analog or Digital Control
- Linearity
- Gain control range
- Noise
- Resolution if digitally controlled

Variable Gain Amplifiers
- Upto 3GHz in operating frequency
- Both digital and analog products
- Linearity, OIP3 upto +31 dBm
- Gain Range:
  - As low as -34dB
  - As high as +22dB
- Noise as low as 4.2dB
- Resolution: Less than 1dB step sizes

AD8370: 700 MHz Digitally Controlled VGA

ADL5330  AD8375-76
AD8368  AD8370

AD8370: 700 MHz Digitally Controlled VGA
Demodulators…
RF Demodulators

Key Design Considerations
- Linearity
- Input Power
- Noise Figure
- Demodulation Accuracy:
  - Phase/Amplitude Balance
- LO to RF Leakage

Broadband Demodulator
- Linearity: IIP3 of +30 dBm
- Input Power: IP1dB of +14dBm
- Noise Figure: 7.8dB
- Phase/Amplitude Balance: <0.5° and <0.25dB
- LO to RF Leakage: -60dBc

www.analog.com/xfest07
ADC Drivers…

Diagram of ADC drivers showing components such as LNA, Mixer, VGA, IQ Mod, ADC Demod, ADC Drivers, DACs, and FPGA, with power management and supervisory functions indicated.
ADC Drivers

Key Design Considerations
- Wide Frequency Range Gain
- Distortion at higher frequencies
- Low noise
- Adjustable Common Mode
- Maintain the performance / quality of the 12- to 16-bit ADC

Ultralow Distortion ADC Drivers
- Wide frequency range gain upto 2GHz
- Distortion specs:
  - 40MHz, -98 dBc HD2 ; -100 dBc HD3;
  - 70MHz, -84dBc HD2; -90dBc HD3
  - 190Mhz, -81dBc HD2  -87dBc HD3
  - Fast settling to 0.01% in less than 8 ns
- Low Input noise density: 2.2nV/√Hz
- Adjustable output common mode voltage
- Low offset voltage – 1mV typical

Ultra Low Distortion
Diff Amp

AD8352 ADA4937-1
ADA4938-1 AD8138
AD8139
ADCs...
ADCs

Key Design Considerations

- Rx Architecture: Direct Down Conversion vs IF sampling
- Signal Bandwidth requirements
- Clock source and desired jitter
- Digital output interface
- Design for manufacturability
Architecture Considerations

- Parameters to consider
  - System sensitivity requirements (Dynamic Range, Gain)
  - Spectrum filtering (analog and digital domains, sample rate)
  - Total cost of BOM, form factor and power consumption

- Dimensions of performance tradeoffs
  - Sensitivity vs signal bandwidth vs cost
Signal Bandwidth and Clocking

- Sampling theory requires at least 2x over sampling of desired signal bandwidth
- SNR performance is a function of input clock jitter and input center frequency
- Trade off
  - SNR over given signal bandwidth vs clock jitter vs input frequency
Digital Interface

- Lot’s of options
  - 1.8V and 3.3V CMOS – single ended, up to 250MHz
  - 1.8v and 3.3V LVDS – differential, up to 800MHz
    - Parallel or serial
    - Single data rate and double data rate modes
    - Other signal controls like over range, synchronization and high Z capable

- Trade off
  - Resulting ADC data rate vs. desired FPGA functionality and I/O availability
# Design for Manufacturability

## Data Sheet Integrity
- Design system to limits, not typs

## Serial Interface Port for User Controls

## Evaluation Tools and Modeling
- Reduces risk and improves time to market

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### AD9230 with V4 Based ADI Data Capture Card

### ADIsimADC Modeling

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**Serial Port Control**—Standard serial port interface supports various product functions, such as data formatting, disabling the clock duty cycle stabilizer, power-down, gain adjust, and output test pattern generation.
ADI’s Large Portfolio of High Speed ADCs

16 bits
- AD9245-20
- AD9248-20
- AD9240 (10)

14 bits
- AD9235-20
- AD9237-20
- AD9238-20
- AD9221 (1)
- AD9223 (3)
- AD9220 (10)
- AD9225

12 bits
- AD9201
- AD9200

10 bits
- AD9201
- AD9200

8 bits
- AD9280
- AD9281
- AD9288-40

DC
- AD9280
- AD9281
- AD9288-40

20 MSPS
- AD9244-20
- AD9245-20
- AD9246-20
- AD6644-40

40 MSPS
- AD9244-40
- AD9245-40
- AD9248-40
- AD6644-40

65 MSPS
- AD9244-65
- AD9245-65
- AD9248-65
- AD6644-65

80 MSPS
- AD9244-80
- AD9245-80
- AD9246-80
- AD9640-80

105 MSPS
- AD9244-105
- AD9246-105
- AD9444-105
- AD9640-105

210 MSPS
- AD9245-125
- AD9246-125
- AD9445-125
- AD9640-125

Future
- AD9244-40
- AD9245-40
- AD9248-40
- AD6644-40

Future
- AD9244-65
- AD9245-65
- AD9248-65
- AD6644-65

Future
- AD9244-80
- AD9245-80
- AD9246-80
- AD9640-80

Future
- AD9244-105
- AD9246-105
- AD9444-105
- AD9640-105

Future
- AD9245-125
- AD9246-125
- AD9445-125
- AD9640-125

Future
- AD9244-40
- AD9245-40
- AD9248-40
- AD6644-40

Future
- AD9244-65
- AD9245-65
- AD9248-65
- AD6644-65

Future
- AD9244-80
- AD9245-80
- AD9246-80
- AD9640-80

Future
- AD9244-105
- AD9246-105
- AD9444-105
- AD9640-105

Future
- AD9245-125
- AD9246-125
- AD9445-125
- AD9640-125
DACs…
**Key Design Considerations**
- Architecture: Direct Up conversion versus IF synthesis
- Frequency planning
- Signal Bandwidth requirements
- Digital Input interface and timing and analog domain adjustments
Types of Architectures

- **Parameters to consider**
  - System Spectral requirements (adjacent channel leakage)
  - Signal synthesis (modulation type, bandwidth, placement)
  - Total cost of BOM, form factor and digital processing complexity

- **Dimensions of performance tradeoffs**
  - Spectral purity vs signal bandwidth vs cost
Frequency Planning and Signal Bandwidth

- Shannon theory
  - Rule of thumb: Digital signal bandwidth less than 40% of update rate
- Placement of analog output is critical relative to clock signals on board
  - Spurs, images, harmonics
- Trade off between input data rate vs signal bandwidth
  - Interpolation and modulation modes moves up in frequency at expense of bw, improves “SNR” in baseband set up

- Spectral content from digital domain
- Sinx/x effect of DAC, overlayed on harmonics from digital domain

Digital -> DAC -> Analog
Digital Interface and Timing and Analog Domain adjustments

- Lot’s of options
  - 1.8V and 3.3V CMOS – single ended, up to 250MHz
    - Multi ports
  - 1.8V and 3.3V LVDS – differential, up to 1200MHz
  - High rates pose huge challenge
    - Sync signals are needed for correct capture of input data
    - Multi-chip synchronization

- Analog Interface options
  - Dual DACs support I&Q Gain, Offset and Phase adjustments
  - Common mode adjustment on single
  - Full scale adjustment

AD9736

AD9779
## TxDAC™ Family D/A Converters

<table>
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<th>Speed (MSPS)</th>
<th>10 to 99</th>
<th>100 to 499</th>
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Over 42 types of TxDACs

[www.analog.com/xfest07](http://www.analog.com/xfest07)
RF Modulators…
RF Modulators

Key Design Considerations
- Linearity (IP3)
- Output P1dB
- Noise Floor
- Quadrature/Amplitude Balance
- Sideband Suppression
- LO to RF Leakage

New Family of IQ Modulator and Broadband Modulator
- Frequency ranging from 50MHz to 4GHz
- OIP3 of +26dBm
- P1dB >10dBm at 3.9GHz.
- Noise Floor -158dBm/Hz
- Sideband Suppression -40dBc
- LO to RF Leakage -40 dBm

Latest Family of Mods
- ADL5370-74
- ADL5385

Broadband Modulator

ADL5370-74

ADL5385
PLL...
PLLS

Key Design Considerations
- Lowest phase noise
- Fast lock time
- Low reference spurious
- Higher Integration for lower cost

Industry’s Highest Performance PLL’s
- As low as -219dBC/Hz phase noise
- Ultra fast locking times (5us)
- Low spurious achievable
- ADIsimPLL free software is industry leader
- New series of PLL with integrated VCO
  - 65MHz – 2.7GHz
Clock Generation and Distribution

Key Design Considerations
- Phase noise / Jitter
- Channel Count
- Timing “Robustness”

Integrated VCO Clock Generator and Distribution
- First 14-output clock generators with integrated VCO to achieve less than 1 picosecond rms jitter
- Six LVPECL outputs
- Four/Eight LVDS/CMOS outputs
- Dual inputs with switchover and holdover capability
- Packaged in 64 LFCSP

AD9516-0, -1, -2, -3, -4

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Power Control…
### Power Control

**Log and RMS Detectors**

#### Key Design Considerations
- Dynamic Range
- Frequency Range
- Temperature Stability
- Linearity
- Modulation independence measurements

#### 3rd Gen Log Amps and Industry’s only true power RMS detectors
- From 30dB to 100dB dynamic range
- Spanning the widest frequency range: LF to 10GHz
- Accuracy from $\pm 0.5$dB
- Temperature stability from $\pm 0.05$
- Industry’s only RF RMS TruPwr Detector

- AD8317
- ADL5519 (Dual)
- AD8318
- AD8361
- AD8362
- AD8364
Key Takeaways

- Entire wireless signal chain
- Architecture agnostic solutions
- Pushing the performance limits, addressing the design challenges

Don’t Forget: http://www.analog.com/xfest07

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